WHAT IS CLAIMED IS:

1. A semiconductor device having a test mode, comprising:

an external input terminal for receiving as an input an external test signal in said test mode;

a selecting circuit selecting any of a plurality of internal signals of said semiconductor device in accordance with a test signal input through said external input terminals;

a plurality of gate circuits provided corresponding to said plurality of internal signals respectively, each receiving a corresponding internal signal at an input node, and applying the corresponding internal signal to an output node in response to selection of the corresponding internal signal by said selecting circuit;

a signal transmission line connected to the output nodes of said plurality of gate circuits; and

an external output terminal for externally outputting the internal signal applied to said signal transmission line.

2. The semiconductor device according to claim 1, wherein each gate circuit includes a tristate buffer setting said output node to a logic level same as the logic level of the corresponding internal signal when the corresponding internal signal is selected by said selecting circuit, and sets said output node to a high impedance state when the corresponding internal signal is not selected.

3. The semiconductor device according to claim 1, wherein

said plurality of gate circuits are divided into a plurality of groups in advance;

said selecting circuit includes

a designating circuit for designating any of said plurality of groups in accordance with a group designating signal included in said test signal, and

a shift register provided corresponding to each group, taking a

plurality of data signals included in said test signal in response to designation of the corresponding group by said designating circuit, and applying the taken plurality of data signals to control nodes of a plurality of gate circuits belonging to the corresponding group, respectively and

each gate circuit applies the corresponding internal signal to said output node when the data signal applied to the control node has an active level, and does not apply the corresponding internal signal to said output node when said data signal has an inactive level.

4. The semiconductor device according to claim 3, wherein

said signal transmission line and said external output terminal are provided same in number as the number of groups of said gate circuits;

the plurality of said signal transmission lines are provided corresponding to said plurality of groups, respectively, each signal transmission line being connected to an output node of each of the gate circuits belonging to the corresponding group;

a plurality of said external output terminals are provided corresponding to said plurality of signal transmission lines, respectively, each external output terminal provided for externally outputting the internal signal applied to the corresponding signal transmission line; and

said designating circuit designates one or more groups among said plurality of groups in accordance with said group designating signal.

5. A semiconductor device having a test mode, comprising:

an external input terminal receiving as an input an external test signal in said test mode;

a first selecting circuit selecting one or more of a plurality of first internal signals of said semiconductor device in accordance with the test signal input through said external input terminal;

a signal generating circuit generating a plurality of first data signals corresponding to said plurality of first internal signals respectively in accordance with said test signal;

a plurality of first gate circuits provided corresponding to said

plurality of first internal signals respectively, each receiving at a first input node, the corresponding first internal signal and at a second input node, the corresponding first data signal, applying the corresponding first data signal to an output node when the corresponding first internal signal is selected by said first selecting circuit, and applying the corresponding first internal signal to said output node when the corresponding first internal signal is not selected; and

an internal circuit performing a prescribed operation based on an output signal of said plurality of first gate circuits.

6. The semiconductor device according to claim 5, wherein

said plurality of first gate circuits are divided into a plurality of first groups in advance;

said first selecting circuit includes

a first designating circuit designating one or more of said plurality of first groups in accordance with a first group designating signal included in said test signal, and

a first shift register provided corresponding to each of the first groups, taking a plurality of second data signals included in said test signal in response to designation of the corresponding first group by said first designating circuit, and applying the taken plurality of second data signals to control nodes of a plurality of first gate circuits belonging to the corresponding first group, respectively;

said signal generating circuit includes a second shift register provided corresponding to each of the first groups, taking a plurality of the first data signals included in said test signal in response to designation of the corresponding first group by said first designating circuit, and applying the taken a plurality of first data signals to second input nodes of the plurality of first gate circuits belonging to the corresponding first group, respectively; and

each of the first gate circuits applies the corresponding first data signal to said output node when the second data signal applied to the control node has a first logic level, and applies the corresponding internal signal to

said output node when said second data signal has a second logic level.

7. The semiconductor device according to claim 5, further comprising:

a second selecting circuit selecting any of a plurality of second internal signals generated by said internal circuit in accordance with said test signal;

a plurality of second gate circuits provided corresponding to said plurality of second internal signals respectively, each receiving at an input node the corresponding second internal signal and applying the corresponding second internal signal to an output node in response to selection of the corresponding second internal signal by said second selecting circuit;

a signal transmission line connected to the output nodes of said plurality of second gate circuits; and

an external output terminal for externally outputting the second internal signal applied to said signal transmission line.

8. The semiconductor device according to claim 7, wherein each of the second gate circuits includes a tristate buffer setting said output node to a logic level same as the logic level of the corresponding second internal signal when the corresponding second internal signal is selected by said second selecting circuit, and sets said output node to a high impedance state when the corresponding second internal signal is not selected.

9. The semiconductor device according to claim 7, wherein

said plurality of second gate circuits are divided into a plurality of second groups in advance;

said second selecting circuit includes

a second designating circuit designating any of said plurality of second groups in accordance with a second group designating signal included in said test signal, and

a third shift register provided corresponding to each of the second

groups, taking a plurality of third data signals included in said test signal in response to designation of the corresponding second group by said second designating circuit, and applying the taken plurality of third data signals to control nodes of a plurality of second gate circuits belonging to the corresponding second group, respectively and

each of the third gate circuits applies the corresponding second internal signal to said output node when the third data signal applied to the control node has an active level, and does not apply the corresponding second internal signal to said output node when said third data signal has an inactive level.

10. The semiconductor device according to claim 9, wherein

said signal transmission line and said external output terminal are provided same in number as the number of groups of said second gate circuits;

the plurality of said signal transmission lines are provided corresponding to said plurality of second groups, respectively, each signal transmission line being connected to an output node of each of the second gate circuits belonging to the corresponding second group;

the plurality of said external output terminals are provided corresponding to said plurality of signal transmission lines, respectively, each external output terminal provided for externally outputting the second internal signal applied to the corresponding signal transmission line; and

said second designating circuit designates one or more of said plurality of second groups in accordance with said second group designating signal.